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The <00l>-oriented growth of Cu_2S films and its switching properties

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Abstract Cu_2S films have been deposited on $Pt/TiO_2/SiO_2/Si(111)$ substrates, and annealed at different temperatures in a vacuum chamber. They were characterized by using X-ray diffraction and scanning electron microscopy. It was observed that the Cu_2S films deposited at room temperature are well crystallized and the grains are oriented along different directions. With the increase of the annealing temperature, the grains of Cu_2S films prefer the <00l>-orientations, and the average size of Cu_2S films decreases. After annealed at 400°C, the films are completely <00l>-oriented, and the grain boundaries of Cu_2S films become undistinguishable due to the possible movements of the ions at high temperature. The resistive ratio of the 'off' state to the 'on' state is about 10^7 for the memory unit of $Cu/Cu_2S/Pt$ structure with the Cu_2S films annealed at 400°C, about 6 orders of magnitude higher than that for the memory unit with the Cu_2S films deposited at room temperature.

Keywords Film growth · Solid state electrolyte · Switching property

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1 Introduction

Bistable conductivity switching phenomenon controlled by external currents or external voltages have attracted much attention due to their potential applications for nonvolatile memory devices [1]. Up to now, this kind of switching behavior has been found in many materials, such as in $SrTiO_3$, NiO, Cu_xO, TiO_2, $La_{1-x}Sr_xMnO_3$ etc., although their working mechanisms may be different due to their unique material systems [2–7]. The large resistive ratio of the so-called 'off' state to the 'on 'state is quite favorable because of the need of a high signal-to-noise ratio for this kind of memory devices. Recent research works on the memory devices based on the solid electrolytes(the so-called 'fast ion conductor'), such as Ag_2S, Cu_xS and $RbAg_4I_5$, etc., show that the large off/on ratio of the resistivity could be obtained [8–10]. The conductance switching of these memory units was ascribed to the creation or the annihilation of the conducting paths(nano-metal filaments) in chalcogenide films formed through the electrochemical reaction between the reactive electrode and the chalcogenide film as well as the non-reactive electrode and the chalcogenide film. When a positive pulse higher than the positive threshold value was applied on the reactive electrode, the metal atoms of the reactive electrode will be oxidized and migrates to chalcogenide film. Correspondingly, the metal ions in chalcogenide film will be reduced at the interface between the chalcogenide film and the non-reactive electrode, and the metal atoms will deposit at the non-reactive electrode. Further, the conducting paths of metal atoms will be created inside the chalcogenide film. In this case, the memory unit should be at the 'on' state. If a negative pulse with the amplitude higher than that of the negative threshold pulse, the metal ions of chalcogenide film will be reduced at the interface

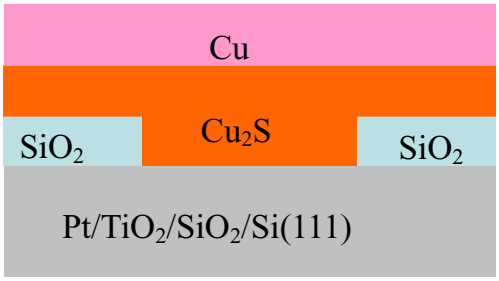

Fig. 1 The schematic structure of Cu_2S memory device

between chalcogenide film and the reactive electrode, and migrates to the reactive electrode. Correspondingly, the metal atoms of the conducting paths will be oxidized and migrates to chalcogenide film. Further, the conducting paths inside chalcogenide film will be broken. In this case, the memory unit should be at the 'off' state. Generally, the chalcogenide films, such as Cu_xS, were prepared by using the electrochemical process [8]. First, the metal films Cu were formed on the substrates through a process of electrodeposition, and then the metal films will be sulfidized in Na_2S solution. The electrochemical process and the composition of the films were very difficult to control, thus the films with pure phase of chalcogenide could not be obtained easily. Here we demonstrate the <00l>-oriented growth of Cu_2S films deposited by using the pulsed laser deposition(PLD) technique. PLD technique has been proven to be a powerful tool to grow films of a wide range of materials, especially the multicomponent compounds. It is also known that the composition of the films deposited by PLD is close to that of the target in spite of some shortcomings, such as the 'droplets' on the surface of the films. We know that the chalcogenide film is hard to be etched in solution or 'drily', so the 'lift-off' lithographic technology is preferred for the fabrication of chalcogenide-based memory devices. Here, to be compatible with the 'lift-off' technology, the Cu_2S films were deposited at room temperature, and then annealed at different temperatures.

2 Experimental

The pure Cu_2S target was employed for PLD process, which was prepared at 600°C with pure Cu_2S powders sealed in a vacuum quartz tube. The Cu_2S target was ablated by a KrF excimer laser(Compex 201, Lambda Physik, 248 nm in wavelength). At a repetition rate of 3 Hz, the laser beam with an average energy density of about 2.0 J/cm^2 was focused at a 45° angle onto the target, which was 8 cm away from the substrate. The Cu_2S films were deposited on $Pt/TiO_2/SiO_2/Si(111)$ substrates, and then annealed at 200, 300 and 400°C, respectively. The structure of the films was determined by using X-ray diffraction with Cu-Kα radiation, and the surface morphology of the film and the cross-section morphology of the heterostructures were observed by using scanning electronic microscopy (SEM). The electric properties of the films were tested by using a Keithley 236 source-measure unit. For testing the electric switching property of Cu_2S films, a memory device of the structure $Cu/Cu_2S/Pt/TiO_2/SiO_2/Si(111)$ was employed. For separating the memory unit with each other, $Pt/TiO_2/SiO_2/Si(111)$ substrates were covered with a 200-nm SiO_2 layer by using plasma enhanced chemical vaporation deposition (PECVD) technique before the deposition of Cu_2S films. Then 25 holes with a diameter of 300 nm in a substrate with the dimension of 10×10 mm^2 were drilled to expose the bottom electrode Pt by using the focused ion beam (FIB) technique (FEI, Strata FIB201). The top electrode Ag was prepared by using dc sputtering technique. The device structure is schematically drawn in Fig. 1.

Figure 2 shows X-ray diffraction patterns of the Cu_2S films deposited on $Pt/TiO_2/SiO_2/Si(111)$ substrates by using PLD technique at room temperature and annealed at 200, 300 and 400°C for 30 min, respectively. For clarity, the diffraction intensity was plotted in a logarithmic scale. At room temperature the deposited films are well crystallized with pure Cu_2S phase, and mainly oriented along <101>-direction as well as <002>- and <004>-directions. When annealed at 200°C for 30 min, the intensity of the (101)-diffraction peak decreases a little, and those of the (002)- and (004)-diffraction peaks increase. After annealed at

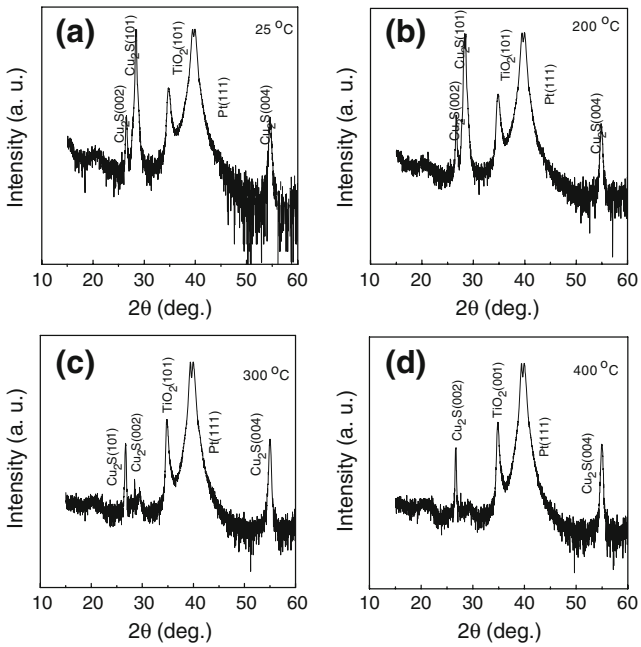

Fig. 2 X-ray diffraction patterns of the Cu_2S films deposited on $Pt/TiO_2/SiO_2/Si(111)$ substrates by using PLD technique at room temperature (**a**), and annealed at 200°C (**b**), 300°C (**c**) and 400°C (**d**), respectively

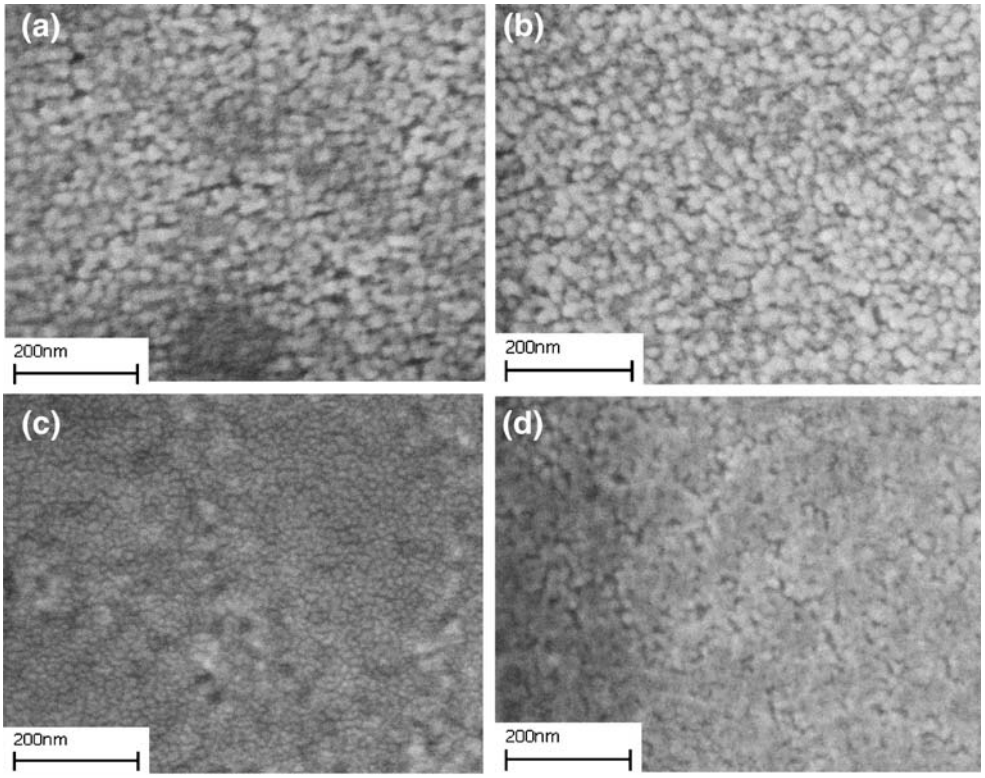

Fig. 3 SEM surface morphology of the Cu_2S films deposited on $Pt/TiO_2/SiO_2/Si(111)$ substrates by using PLD technique at room temperature (**a**), and annealed at 200°C (**b**), 300°C (**c**) and 400°C (**d**) for 30 min, respectively

300°C for 30 min, the Cu_2S films were mainly oriented along <002>- and <004>-directions. After annealed at 400°C for 30 min, the Cu_2S films were completely oriented along <002>- and <004>-directions.

Figure 3 shows the SEM morphologies of the Cu_2S films deposited on $Pt/TiO_2/SiO_2/Si(111)$ substrates by PLD at room temperature and annealed at 200, 300 and 400°C for 30 min, respectively. The Cu_2S films deposited at room temperature were well crystallized, consistent with the results of X-ray diffraction patterns as shown in Fig. 2. The surface of Cu_2S film is very flat and the average size of the Cu_2S grain particles is about 20 nm. When annealed at 200°C for 30 min, the average size of the Cu_2S films decreases a little. After annealed at 300°C for 30 min, the average size of the Cu_2S grains become much smaller, and the films seem denser. Finally, after annealed at 400°C for 30 min, the contour of the Cu_2S grain particles and the grain boundaries become undistinguishable. This phenomenon may be ascribed to the improved mobility of ions in Cu_2S films at higher temperature. At high temperature, the solid electrolyte Cu_2S shows a good ionic conductivity, which is from the hoping movements of Ag^+ ions inside the electrolyte. Because of the high mobility of ions in Cu_2S, the neighboring grain particles are easy to merge together to reduce the surface energy, thus resulting in the unclear grain boundaries. On the other hand, the high annealing temperature (400°C) also may result in the decomposition of Cu_2S films partly, thus a sulphur-deficient film develops. Further studies on the microstructures of the annealed Cu_2S films is continued. Figure 4 shows the SEM cross-section morphology of the heterostuctures $Cu_2S/Pt/TiO_2/SiO_2/Si$ (111). The thickness of Cu_2S film was determined as about 80 nm.

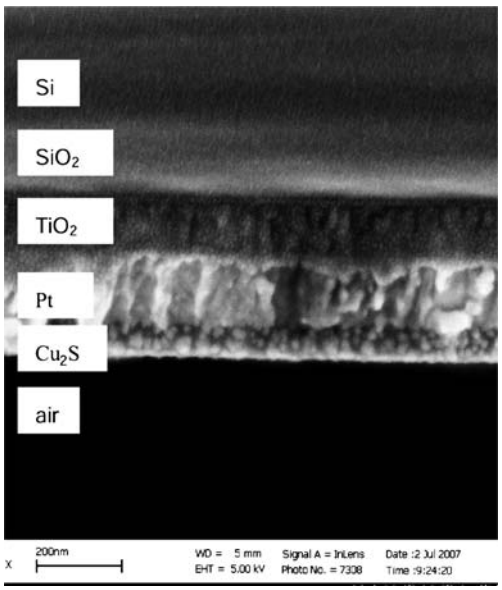

Fig. 4 SEM cross-section morphology of the heterostuctures $Cu_2S/Pt/TiO_2/SiO_2/Si(111)$

To investigate the effect of the microstructures of the Cu_2S films on its switching properties, the measurements on the I–V characteristics of the heterostructures $Cu/Cu_2S/Pt/TiO_2/SiO_2/Si(111)$ as deposited at room temperature and

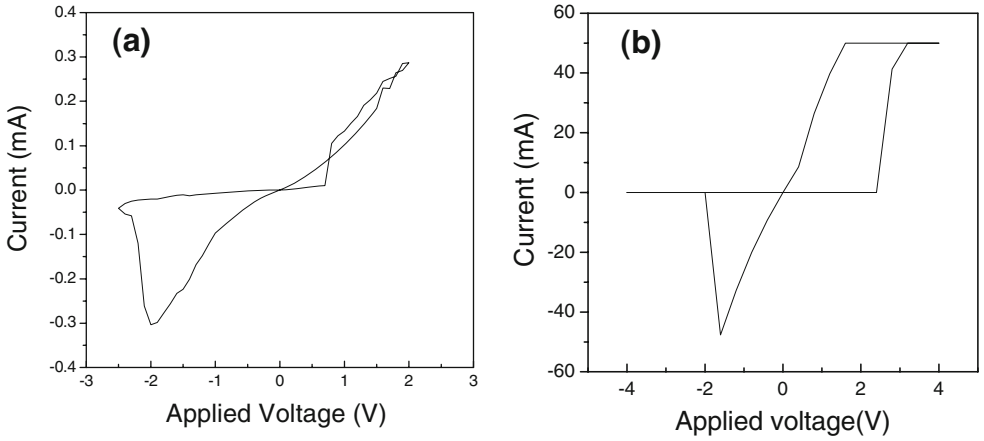

Fig. 5 The I–V characteristics for the heterostructures Cu/Cu_2S/Pt/TiO_2/SiO_2/Si(111) unannealed (**a**) and annealed at 400°C (**b**)

annealed at 400°C were both performed, as shown in Fig. 5(a) and (b). Both figures show clear resistive switching behaviors of Cu_2S memory units. The possible switching mechanism should be ascribed to the formation and the annihilation of Cu filaments in Cu_2S films, similar with that suggested by Hasegawa and co-workers [8]. From Fig. 5(a), the positive threshold voltage, which turns the Cu_2S memory unit with unannealed heterostructures Cu/Cu_2S/Pt/TiO_2/SiO_2/Si(111) from the 'off 'state to the 'on' state, is about 0.7 V, and the resistance of the 'on' state is determined as 7.0×10^3 Ω.

The negative threshold voltage, which turn the memory unit from the 'on' state to the 'off' state is about −2 V, and the resistance of the 'off' state is determined as 8×10^4 Ω. So the resistive ratio of the memory unit with the unannealed Cu_2S film between the 'off' state and the 'on' state is about 10. After Cu_2S films were annealed at 400°C for 30 min, the switching properties of the Cu_2S memory unit were improved greatly, as shown in Fig. 5(b). The positive threshold voltage for the Cu_2S memory unit annealed at 400°C is about 2.4 V, and the resistance of the 'on' state is determined as about 30 Ω, much lower than that of the 'on' state for the unannealed memory unit. This should be ascribed to the improvement of the microstructure of the annealed Cu_2S films and the interface between Pt and Cu_2S as well as Cu and Cu_2S due to the annealing process. From Fig. 5(b), the negative threshold voltage for the memory unit is about −1.6 V, and the resistance of the 'off' state is about 3×10^8 Ω, much higher than that of the 'off' state for the unannealed memory unit. This should be attributed to the reduction of the grain boundaries in the annealed Cu_2S films due to the annealing process, which is the main origin of the leakage current of the memory unit. The resistive ratio of the annealed memory unit between the 'off' state and the 'on' state is about 10^7, six orders of magnitude larger than that of the unannealed memory unit. It is also obvious from Fig. 5(a) and (b). that the I–V behaviors in the 'on' states between the unannealed Cu_2S memory unit and the annealed Cu_2S memory unit are quite different. For the unannealed Cu_2S memory unit as shown in Fig. 5(a), the I–V behavior in the 'on' state in the region of the applied voltage 2 V to −2 V is not linear, which should be attributed to the bad interface between Pt and Cu_2S as well as Cu and Cu_2S, thus the barriers of the charge carriers was formed. While the annealed Cu_2S memory unit shows a good linear behavior in its I–V characteristics in the region of the applied voltage 1.6 V to −1.6 V, which should be attributed to the disappearance of the barriers at the interfaces due to the annealing process.

It is reasonably concluded that the post-annealing process after the deposition of Cu_2S films by using PLD technique will effectively reduce the grain boundaries, and improve the microstructures of Cu_2S films and the interface of Cu_2S memory unit, thus enhancing the switching properties of Cu_2S memory unit.

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